Disclaimers

The SPICE model provided by Innoscience describes the typical electrical behavior of InnoGaN devices. Although model simulation can effectively evaluate the behavioral characteristics of the device during switching and improve the efficiency of the principle design, it cannot completely cover the actual working conditions of the device. The verification of the breadboard is still necessary.

At present, Innoscience provides four model files: **LTspice, Pspice, SIMetrix, and Spectre**. In the future, other types of models will be added as required. Innoscience reserves the right to update the model, and the model files will be updated without notice.

The simulation model cannot accurately reflect the device performance under all conditions, nor can they replace the breadboard for final verification.

If you have any questions during the use of the SPICE model, please feedback to us. Your help is the driving force for Innoscience to move forward.

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Table of Contents

Introduction

1 InnoGaN Modelling Levels

The InnoGaN SPICE model provided by Innoscience is divided into three levels, LV1 model, LV2 model, and LV3 model.

- The LV1 model only contains the basic behavioral characteristics of the device. The LV1 model is widely used in simulation work at present with its fast simulation speed and easy convergence. LV1 model can also set a constant junction temperature parameter Tj to evaluate the effect of temperature on device behavior.

- The LV2 model adds the parasitic parameters of the package. The parasitic parameters are obtained through physical simulation. The LV2 model can effectively estimate the electrical stress during the use of the device.

- The LV3 model is based on the LV2 model by adding an RC thermal resistance network. The LV3 Model can evaluates the coupling relationship between self-heating caused by power dissipation and its electrical behavior characteristics.

2 InnoGaN SPICE Model Library Files

Innoscience provides four types of model library files, LTspice, Pspice, SIMetrix, Spectre. The model file details are shown in Table 1.

Table 1 Introduction to model files

File	Simulator	Remark
*_LTspice.lib	LTspice	associate with the *.asy file
*_PSPICE.lib	OrCAD	auto generate *.olb file
*_SIMetrix.lib	SIMetrix	associate with the .*sxslb file
*_Spectre.scs	virtuoso	auto generate *.oa file

3 InnoGaN SPICE Model Architecture

The basic architecture of InnoGaN SPICE model is shown in Figure 1, which is similar to the equivalent sub-circuit model of traditional silicon devices.

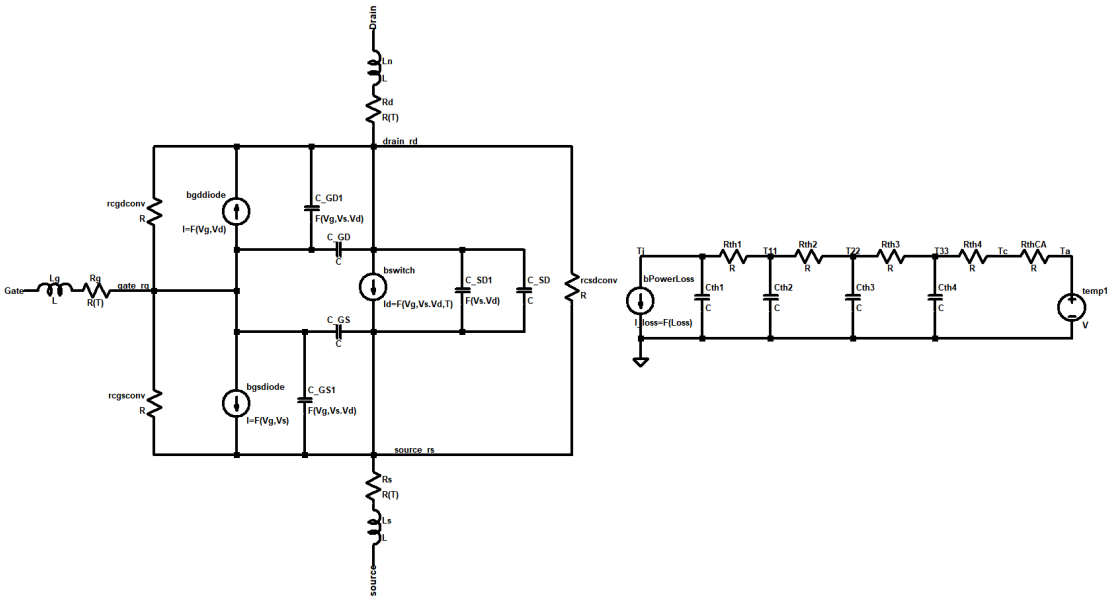

Fig.1. InnoGaN equivalent subcircuit model

Main channel current Id： Bswitch is an arbitrary current source, used to simulate the behavior of the main channel of the device. When Vds>0, Id is positive and flows from the drain to the source; when Vds<0, Id is negative and flows from the source to the drain. The main channel current Id is affected by the source, drain, gate voltage and temperature.

CGS capacitor： It is composed of static capacitance C_GS and non-linear capacitance C_GS1. Among them, C_GS is the equivalent capacitance between the gate and the source metal plate, which is generally regarded as a constant value. C_GS1 is the equivalent capacitance between the gate and the main channel on the source side, and its value is affected by the source-drain gate voltage.

CGD capacitor： It is composed of static capacitance C_GD and non-linear capacitance C_GD1, where C_GD is the equivalent capacitance between the gate and the drain metal plate, which is generally considered to be a constant value. C_GD1 is the

equivalent capacitance between the gate and the main channel on the drain side, and its value is affected by the source-drain gate voltage.

CSD capacitor： It is composed of static capacitance C_SD and nonlinear capacitance C_SD1, where C_SD is the equivalent capacitance between the source and drain metal plates, which is generally considered to be a constant value. C_SD1 is the equivalent capacitance between the main channel on the source and drain sides, and its value is affected by the source drain gate voltage.

Rd/Ld Drain parasitic inductance and resistance: Characterizes the parasitic parameters of the drain package of the device, and the Rd value is affected by temperature.

Rs/Ls Source parasitic inductance and resistance: Characterizes the parasitic parameters of the device source package. The Rs value is affected by temperature.

Rg/Lg Gate parasitic inductance and resistance: Characterize the parasitic parameters of the device gate package, the Rg value is affected by temperature.

RC thermal resistance network： It is composed of any current source bPowerLoss and thermal resistance Rth thermal capacity Cth, which is used to simulate the coupling relationship between device self-heating and electrical behavior characteristics. bPowerLoss is an InnoGaN power loss equivalent model, which equates the self-heating power Loss of the device to current, voltage is equivalent to temperature, resistance is equivalent to thermal resistance, and capacitance is equivalent to heat capacity. The corresponding equivalent relationship of the RC thermal resistance network is shown in Table 2 below.

Table 2 RC thermal resistance network mapping relationship

Current - I（A）	→	Power - P（W）
Voltage - V（V）	→	Temperature - T（℃）
Resistance - R（Ω）	→	Thermal resistance -Rth（℃/ W）
Capacitance - C（F）	→	Heat capacity - Cth（J/℃）

LTspice model User Guide

The LTspice model contains *.lib and *.asy files, where *.lib is the model library file, *.asy is the symbol file, and the LV1/ LV2/LV3 symbols are shown in Figure 1 below. LV1 and LV2 models similarly have three external pins as G/D/S, LV3 model has five external pins as G/D/S/Tj/Ta, and its recommended range is shown in Table 1.

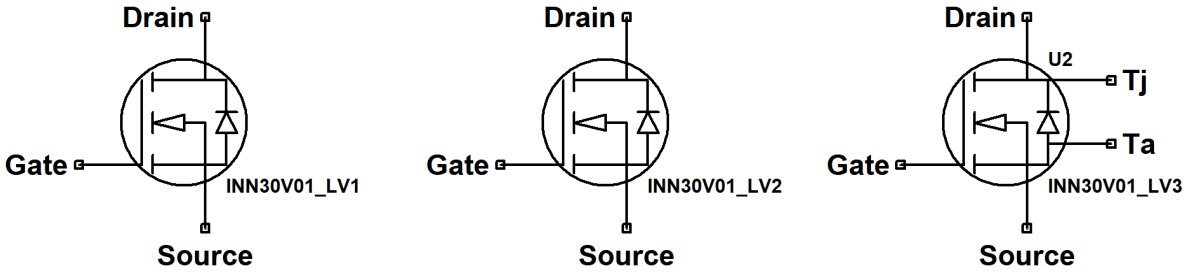

图 1 LV1/ LV2 /LV3 Symbol file and Terminals definition

Table 1 Recommendations for the use of the InnoGaN model

InnoGaN Level	Terminals	Usage suggestion
LV1	G，D，S	Transient, switching losses and efficiency analyses. Behavior of device over full temperature range
LV2	G，D，S	Generally mainly used for electrical stress analysis
LV3	G，D，S，Tj，Ta	Self-heating effects, modeling of heat flow including thermal models of application.

1. **Load the lib file.** Use Notepad or LTspice simulator to open the downloaded InnoGaN *.lib file, which uses an equivalent sub-circuit model to simulate the electrical behavior of InnoGaN. The basic structure is shown in Figure 2 below,

Fig.2. Basic architecture of sub-circuit model

2. **Associate with *asy files**。Open the *.asy file and press the shortcut key Ctrl+A to pop up the dialog box shown in Figure 3 below.

Notice:

- *The number and sequence of the PIN pins of the symbol must be consistent with those in the sub-circuit, and the pin names can be inconsistent;*
- *The model name in schematic must be consistent with the name of the sub-circuit in spice model *.lib file;*
- *The Modelfile name of the symbol must be consistent with the *lib file name;*

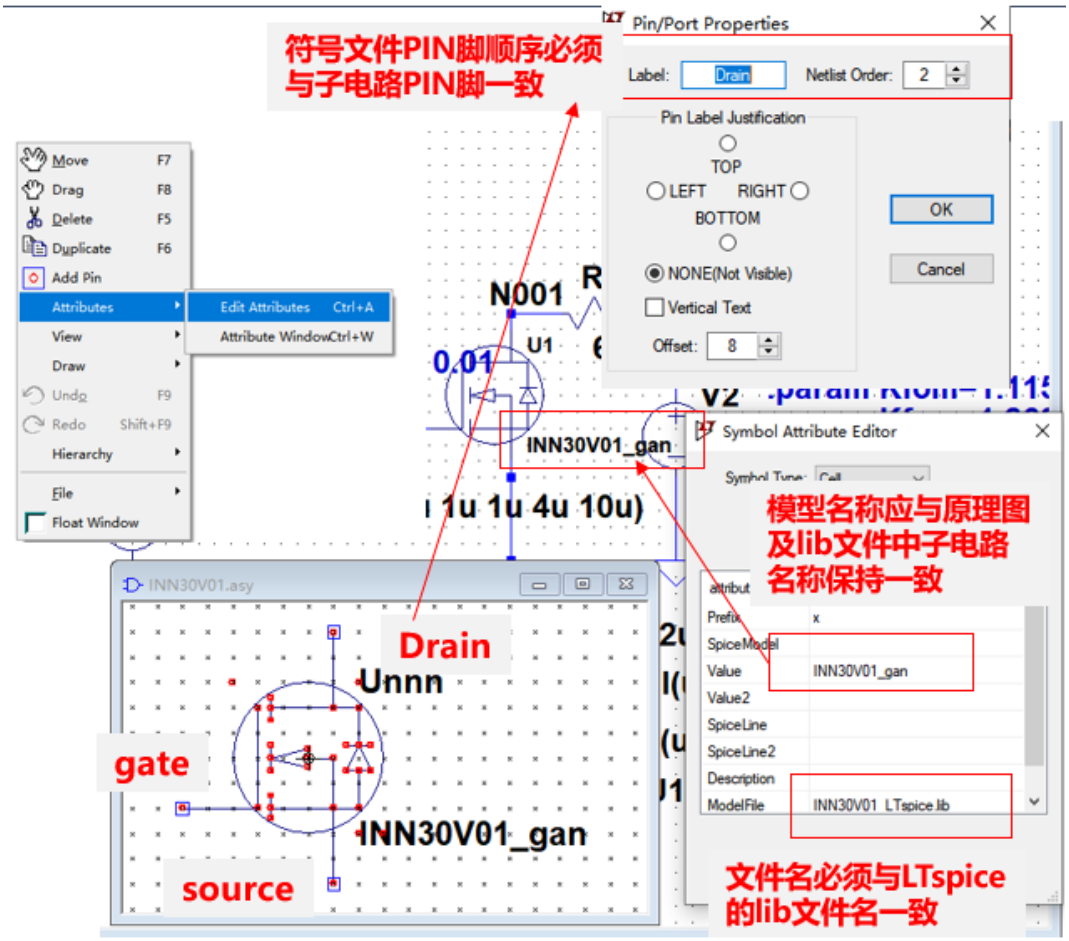

Fig.3. *.lib and *.asy file association

3. **Add InnoGaN model to the schematic.**Generally, InnoGaN provides the associated *.lib and *.asy files, and step 1/2 can be omitted. After association, click the component button in the toolbar on the schematic editing interface as shown in the figure below, or press the shortcut key F2, and a pop-up is shown as shown in the figure. Select the InnoGaN model save path in the Top Directory drop-down box, and select the desired device name in the device selection window, as shown in Figure 4.

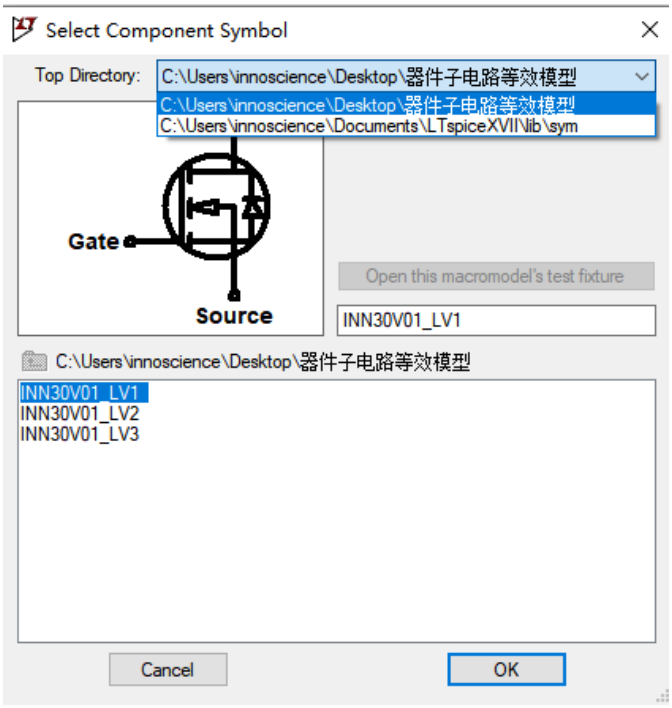

Fig.4. Add the InnoGaN model to the schematic

4. **Set simulation parameters and run.** Set the simulation parameters according to the simulation requirements. The simulation results of the device output curve are shown in Figure 5 below.

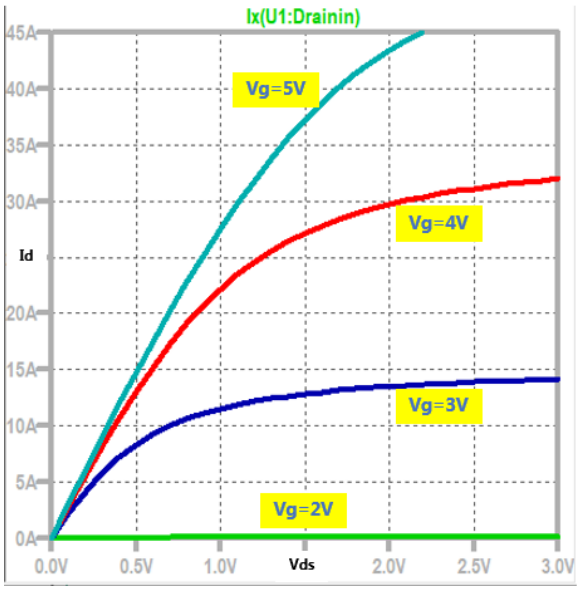

Fig. 5. InnoGaN output LTspice simulation result

Pspice Model User Guide

The Pspice model contains *.lib and *.olb files, where *.lib is the model library file, and *.olb is the symbol file. The Pspice model import process is as follows:

1、 **Load lib file**.
Open Pspice Model Editor ,Click File->open to load the lib file into the editor. To view or edit the model file in the editor, double-click the device name on the left.

2、 **Export olb file**.
Click File->Export to Capture Part Library to export the *.olb file. The erro dialog box pops up, and the export is successful if there is no error.

3、 **Associate lib files and olb files**.
Click File—>Model Import Vizard to pop up a dialog box as shown in the figure below, Click Next> to pop up generation information, OK. At this point, the Spice model is created.

4、 **Add the InnoGaN model to the project file.**
Capture CIS-> Edit Simulation Profile -> Configuration Files -> Load .lib File -> Add to Design—>ok。

5、 **Add InnoGaN to the simulation schematic**.
The steps for adding the InnoGaN model to the Cadence schematic are as follows:Place Part ->Add Library -> Double click InnoGaN model.

6、 **Set the simulation parameters and run**.
Set the simulation parameters according to the simulation requirements, and view the simulation results.

SIMetrix Model User Guide

The SIMetrix model contains *.lib and *. sxslb files, where *.lib is the model library file, and *. sxslb is the symbol file. The SIMetrix model import process is as follows:

1、 **Import lib file。**
File -> Model Library -> Add/Remove Libraries ->
Select Spice File folder -> ok。

2、 **Import Symbol file。**
File -> Symbol Manager -> Add -> Select *.sxslb File -> ok。

3、 **Associate Symbol file。**
File -> Model Library -> Associate models and symbols ->New Category -> Define Symbol -> ok。

4、 **Add to the schematic。**
Place –> From the Library -> : Select InnoGaN and device-> Place。

5、 **Set the simulation parameters and run**.
Set the simulation parameters according to the simulation requirements, and view the simulation results.

Spectre Model User Guide

The Spectre model is used in Virtuoso with the symbol file *.oa. The Spectre model import process is as follows:

1. Create a symbol file
   - Symbol model name must be consistent with model file subckt name；
   - The number and sequence of Symbol PIN pins must be consistent with the subckt definition in the model file, and the pin names can be inconsistent.

2. Create Schematic
   Build a circuit diagram with symbol in the Virtuoso schematic editor window

3. Simulation Setting
   1) Launch -> ADE L -> Pop up ADE L window
   2) Setup –> Simulator/Directory/Host… -> Select simulator as spectre in the pop-up window -> OK
   3) Setup –> Model Libraries -> Import the *_Spectre.scs model file in the pop-up window -> OK

4. Set simulation conditions and view the simulation results.

RC Thermal Resistance Network User Guide

Innoscience LV3 SPICE model provides RC thermal resistance network parameters to simulate electro-thermal coupling simulation. This tutorial uses LTSPICE to simulate a BUCK circuit as an example. The switch uses the Inno650D260A LV3 SPICE model, and the PCB uses the SOAtherm-PCB model, which is to simulate the thermal capacity and thermal resistance of the PCB, Schematic is shown in Figure 1 below. The Tc pin of the InnoGaN is connected to the Tc pin of SOAtherm-PCB.

The PCB parameters:

- PCB Copper Thickness：1 oz;
- Device Pad Area: 21 mm^2;
- PCB Area：2500 mm^2;
- PCB Thickness：1.5 mm;
- Natural convective speed：50 LFM;

The parameters of the BUCK circuit:

- Input voltage：400V;
- Output voltage：200V;
- Load current：4A;
- Switching Frequency：150kHz;
- Ambient temperature：45 ℃;

After the simulation is completed, the thermal-electric coupling simulation waveform and its zoom-in are shown in Figure 2 and Figure 3. In addition to effectively evaluating the steady-state power consumption and steady-state junction temperature of the device, the LV3 level model can also simulate the transient power consumption and transient junction temperature of the device during the switching cycle.

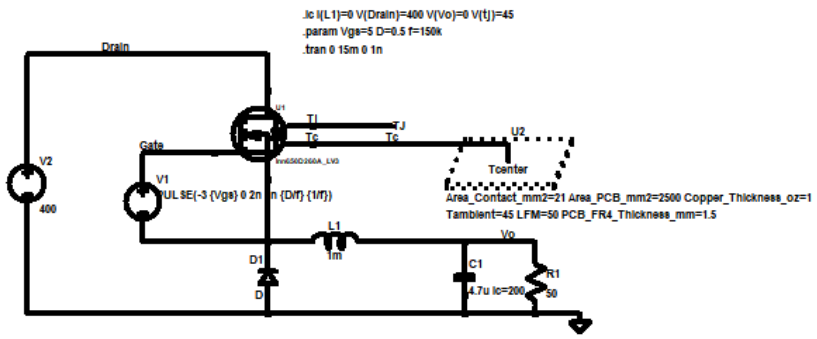

Fig.1. BUCK circuit device electro-thermal coupling simulation schematic diagram

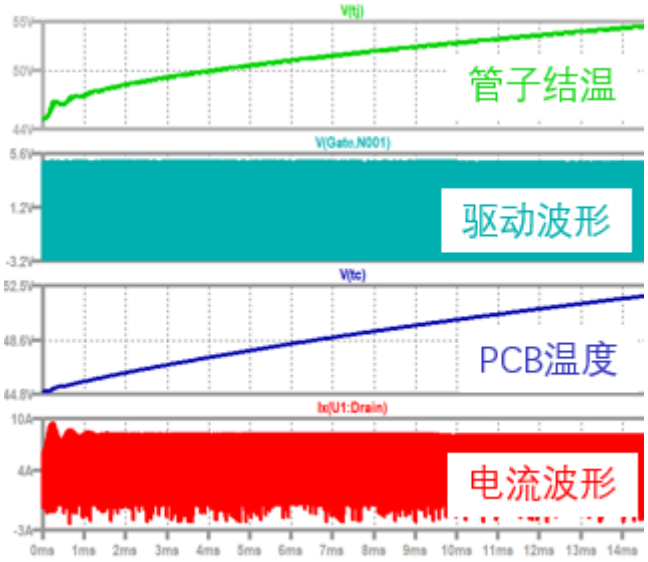

Fig.2. Basic waveform diagram of BUCK electric heating simulation

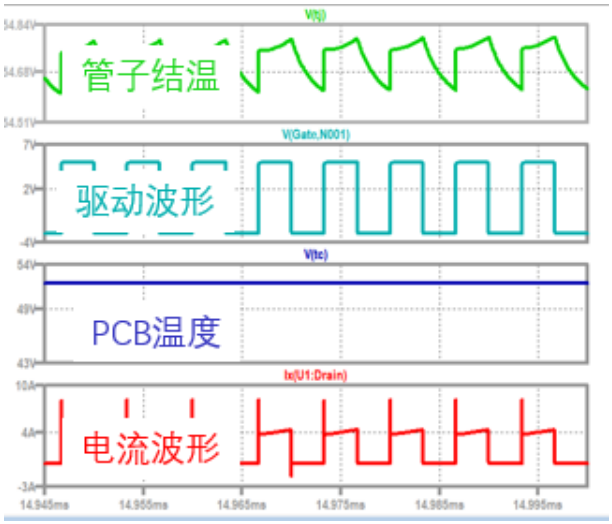

Fig. 3. BUCK Electric heating simulation magnified waveform diagram